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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,512	07/29/2003	Zheng (Jeff) Chen	M-15197 US	6913

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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,512	CHEN ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-8,11-13 and 15-19* is/are rejected.

7)☒ Claim(s) *2,3,9,10,14 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~7-29-2003~~. 12-22-03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1- are rejected under 35 U.S.C. 102(b) as being anticipated by Kean (US PAT No. RE37,195).

Regarding claim 1. Figs. 5 and 6C of Kean teaches a programmable logic device comprising: a system bus (bus 32 in Fig. 5); a plurality of configuration memory cells (38 in Fig. 6C); and a memory interface (21, 26 and BIT0 /BIT0 ... BIT31, /BIT30 in Fig. 6C), coupled to at least configuration memory cells and couplable to the system bus via a programmable interconnect (34 in Fig. 5 and 6C), adapted to provide access to the at least one configuration memory cell after configuration of the programmable logic device to write data carried by the system bus to the at least one configuration memory cell (see Abstract).

Regarding claim 4, Figs. 5 and 6C of Kean teaches the programmable logic device of claim 1 where the at least one configuration memory cell is associated with a special functional block within the programmable logic device (complex function logic being special functional block; col. 5, lines 39-45).

Regarding claim 6, Figs. 5 and 6C of Kean teaches the programmable logic device of claim 1 where the configuration memory cells comprise static random access memory cells and/or flip flops (SRAM, col. 1, lines 33-37).

Regarding claim 7, Figs. 5 and 6C of Kean teaches the programmable logic device of claim 1 where the memory interface communicates with the at least one configuration memory cell in byte increments (access bit or word(byte), col. 8, lines 31-35).

Regarding claim 8, Figs. 5 and 6C of Kean teaches the programmable logic device of claim 1 where a programmable identification number is associated with the memory interface (row and column numbers associated with 38).

Regarding claim 11, Figs. 5 and 6C of Kean teaches a programmable logic device comprising a system bus (bus 32 in Fig. 5); a programmable interconnect (34 in Fig. 5 and 6C); means for storing configuration data; and means for interfacing interface (21, 26 and BIT0 /BIT0 ... BIT31, /BIT30 in Fig. 6C) with the storing means after configuration has completed to change the configuration data stored by the storing means with data carried by the system bus, where the interfacing means is couplable to the system bus via the programmable interconnect (see Abstract).

Regarding claim 12, Figs. 5 and 6C of Kean teaches the programmable logic device of Claim 11, wherein the interfacing means is addressed via one or more programmable identification numbers (row and column numbers associated with 38).

Regarding claim 13, Figs. 5 and 6C of Kean teaches the programmable logic device of claim 11 wherein the storing means comprises static random access memory cells (SRAM, col. 1, lines 33-37).

Regarding claim 15, Figs. 5 and 6C of Kean teaches the programmable logic device of claim 11 where the storing means is associated with a special functional block (complex function logic being special functional block; col. 5, lines 39-45).

Regarding claim 16, Figs. 5 and 6C of Kean teaches a method of modifying configuration data stored within a programmable logic device after configuration has been completed (see Abstract), the method comprising: providing memory interfaces (21, 26 and BIT0 /BIT0 ... BIT31, /BIT30 in Fig. 6C) for a plurality of configuration memory cells which store at least a portion of the configuration data; providing a system bus (bus 32 in Fig. 5) for carrying data to be written to at least some of the plurality of the configuration memory cells; and providing a programmable interconnect (34 in Fig. 5 and 6C) adapted to couple the system bus to the memory interface to route the data from the system bus to the memory interface.

Regarding claim 17, Figs. 5 and 6C of Kean teaches the method of Claim 16, wherein each of the memory interfaces is addressed via an associated programmable identification number (row and column numbers associated with 38).

Regarding claim 18, Figs. 5 and 6C of Kean teaches the method of Claim 17, wherein the programmable identification number may be the same for one or more of the memory interfaces (same row numbers and different column numbers associated with 38).

Regarding claim 19, Figs. 5 and 6C of Kean teaches the method of Claim 16, wherein the plurality of the configuration memory cells are associated with special functional blocks (complex function logic being special functional block; col. 5, lines 39-45).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kean in view of Baxter (US PAT No. 6,675,306).

Regarding claim 5, Figs. 5 and 6C teaches the programmable logic device (e.g. XC4000) of Claim 4, where the special function block being a complex function logic, but does not teach the complex function logic being a phase-locked loop circuit, a delay-locked loop circuit, an input/output circuit, and/or a memory interface controller. However, Baxter teaches an apparatus (XC4000) performing PLL (see ABSTRACT) as a part of application of FPGA. Therefore it would have been obvious to one skilled in the art, at the time of the inventions, to provide a phase-locked loop circuit of Baxter since Baxter shows that it is well known in the art that an FPGA is a programmable by a user defined complex logic circuit such as a phase-locked loop circuit.

Allowable Subject Matter

Claims 2-3, 9-10, 14 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Kean teaches partial configuring FPGA and Baxter teaches an FPGA performing PLL, one of ordinary skill in the art would not have been motivated to modify the teaching of Kean and/or Baxter to further includes, among other things, the specific of a system bus register file coupled to the system bus and couplable to the programmable interconnect providing an interface between the memory interface and the system bus., as set forth in the claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Schultz et al. (US PAT No. 6,255,848) discloses a method and structure for reading modifying and writing selected configuration memory cells of an FPGA.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

October 21, 2004